

Laboratory 3

(Due date : 002/003: October 10th, 004: October 11th)

OBJECTIVES

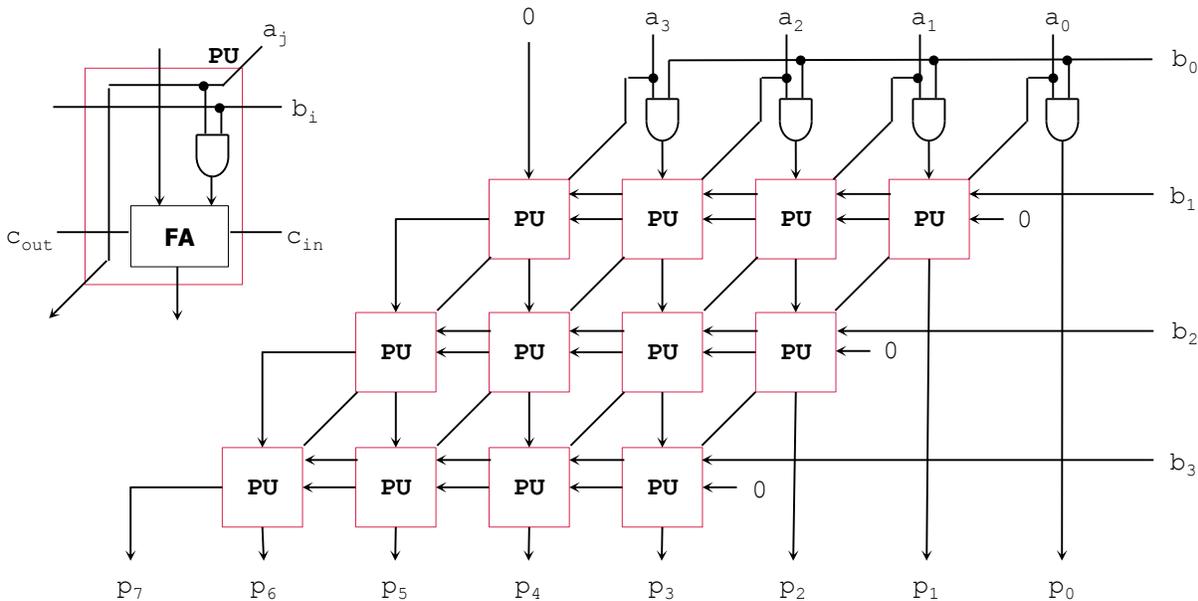
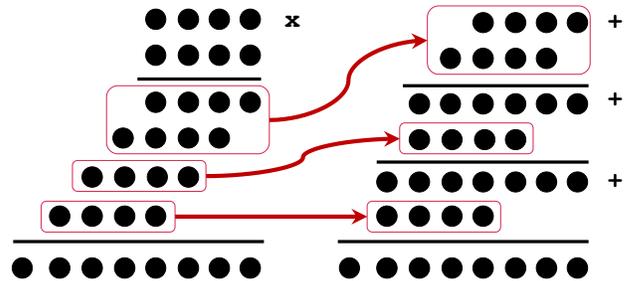
- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

VHDL CODING

- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a list of examples.

FIRST ACTIVITY (100/100)

- **PROBLEM:** An alternative implementation of the multiplication operation is depicted in the figure for 4-bit unsigned numbers. It is much simpler to see how only two rows are added up at each stage.



- ✓ Create a new ISE Project. Select the **XC7A100T-1CSG324 Artix-7 FPGA** device.
 - ✓ Write the VHDL code for the given array multiplier of two unsigned numbers of 4 bits. Use the **Structural Description**: Create a separate file for the Full Adder, the Processing Unit (PU), and the top file (Array Multiplier).
 - ✓ Write the VHDL testbench to test the circuit to test representative cases (or all cases).
 - ✓ Perform **Functional Simulation** and **Timing Simulation** of your design. **Demonstrate this to your TA.**
 - ✓ I/O Assignment: Create the UCF file. Nexys-4: Use SW0 to SW7 for the inputs, and LED7 to LED0 for the output.
 - ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA.**
- Submit ([as a .zip file](#)) the five generated files: VHDL code (3 files), VHDL testbench, and UCF file to Moodle (an assignment will be created). DO NOT submit the whole ISE Project.

TA signature: _____

Date: _____